SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100

APPLICATION NOTE FOR CRT 5027

VTAC

Figure 1 shows the basic configuration for a bus oriented microprocessor based CRT display system utilizing SMC's CRT 5027 (VTAC) and CG5004L-1 (Character Generator). A standard or non-standard CRT TV raster monitor may be used. The user programmable VTAC provides Horizontal Sync, Vertical Sync, Composite Sync and Blanking to the monitor's deflection circuitry. Serial Video Data, at the dot-clock frequency, is supplied to the Z axis (Video input) of the monitor, from the CG5004L-1 on-chip shift register.

In addition to the CRT 5027 and CG5004L-1 the display system requires a crystal oscillator, consisting of two gates of a 7404 and a crystal as well as a dot counter (74160). The dot counter divisor (N) is set for the number of horizontal dots in the character plus the number of dots desired for spacing (ie. for a 7 bit wide character + 2 dots of spacing N = 9). The carry output of the dot counter pulses once per character (character clock) and is fed into the DCC input of VTAC. This enables the VTAC to keep track of the character positions as well as generate the entire video timing chain. At the same time the output of the oscillator is fed into the clock input of the on-chip shift register of the CG5004L-1.

An 8 bit bi-directional data bus (DBØ-7), a 4 bit address bus (AØ-3), a chip select and a data strobe are used in programming the VTAC. These buses connect to the microprocessor data bus and address bus. The VTAC appears to the microprocessor as 16 memory locations. Page logic connects the address bus to the chip select thereby determining where in the microprocessor memory space the VTAC will be located. The data strobe signal is connected to the microprocessor control bus. This is used to read or write via the data bus, as well as to activate control functions.

The VTAC raster scan counter outputs (RØ-3) are connected directly to the line address inputs (L1-4) of the CG5004L-1 character generator. This 4-bit address indicates which raster line of the selected character is to be parallel loaded into the internal shift register. This bit pattern, along with the additional blank spaces, is then shifted out of the serial output (as video) at the dot clock rate. The blanking signal can be ANDed with the video or connected to the clear input of the CG5004L-1. The load signals for the CG5004L-1 can be derived from the outputs of the dot counter (74160).

The VTAC outputs the character position via the character counter outputs (HØ-7) and the data row counter outputs (DRØ-5). These outputs define the character column and row location. They are used to address a character frame buffer RAM in which the frame image is stored.

The character column and character row outputs combine to form the character address bus. This bus, along with the microprocessor address bus, is connected to a 2 X 1 selector which addresses the character frame buffer RAM.

Figure 2A shows an address compression scheme using 80 characters per line and from 12 to 48 lines of data per frame. The CRT 5027 still outputs character column (HØ-6) and the data row (DRØ-5). The microprocessor address bus similarily addresses the row and character locations along with the page location of the character frame buffer memory. As the microprocessor software does not have to go through any algorithms to find an absolute address it can be greatly simplified. The microprocessor control bus operates the selector logic which addresses the character frame buffer. This can be from either the microprocessor address bus or from the CRT 5027 character address bus. The selector logic

may utilize 74LS157's or 257's.

When using 80 characters/line the address bus does not efficiently make use of all RAM locations, as 80 is not a binary number. To correct this a 74184 (BCD to binary converter) is used to encode memory segments in the character frame buffer. This method allows 80 characters per line X 12 lines to be contained within a 1K byte RAM. The least significant 6 bits (AØ-5) come directly from the selector logic and address a 64 byte segment comprised of 16 characters by 4 lines. 15 such segments are required to fill in the 960 characters. The remaining 4 bits (A6-9) are derived from the outputs of the BCD to binary converter (Y1-4). Thus, the 11 lines (HØ-6, DRØ-3) are now converted to a 10 bit address (AØ-9) to address the 1K byte RAM for: 80 characters per line X 12 lines. For more than 12 lines, an additional 74184 can be used to expand the memory address up to 48 lines (4K bytes).

Figure 2B shows a memory map of the RAM (80 character per line X 12 lines). The 15 segments (A-O) are each made up of 16 characters X 4 lines. The 64 bytes within each of the 15 segments are addressed by the low order address bits AØ-A5. The segments are encoded throughout the 1K address space by the 74184 BCD to binary converter. Since the encoding is located after the selector logic, both the microprocessor address algorithms and the CRT 5027 character and row outputs are the same. This scheme greatly simplifies the microprocessor software requirements for locating a character within the memory as well as making much more efficient use of the memory space. This is only one of many possible schemes, there are many other variations for 80 characters as well as other programmable formats of the CRT 5027.

An alternate memory mapping circuit is shown in Figures 2C, 2D, and 2E. It maps 72 or 80 characters/line X 12,24 or 48 lines into 1K, 2K or 4K bytes.

The character frame buffer RAM is initially loaded via the microprocessor data and address busses (see Figure 1). After the microprocessor has loaded the character frame buffer RAM with a complete page, the selector is switched (via the microprocessor control bus) so that the RAM is addressed by the character address bus of the VTAC. In this mode the VTAC operates independent of the microprocessor by addressing the character frame buffer RAM which sends the ASCII data to the CG5004L-1 character generator. The selected character is then further decomposed by the raster scan counter, from the VTAC, and loaded into the internal shift register of the CG5004L-1. This bit pattern is then serially shifted out at the video dot clock frequency so as to form serial video.

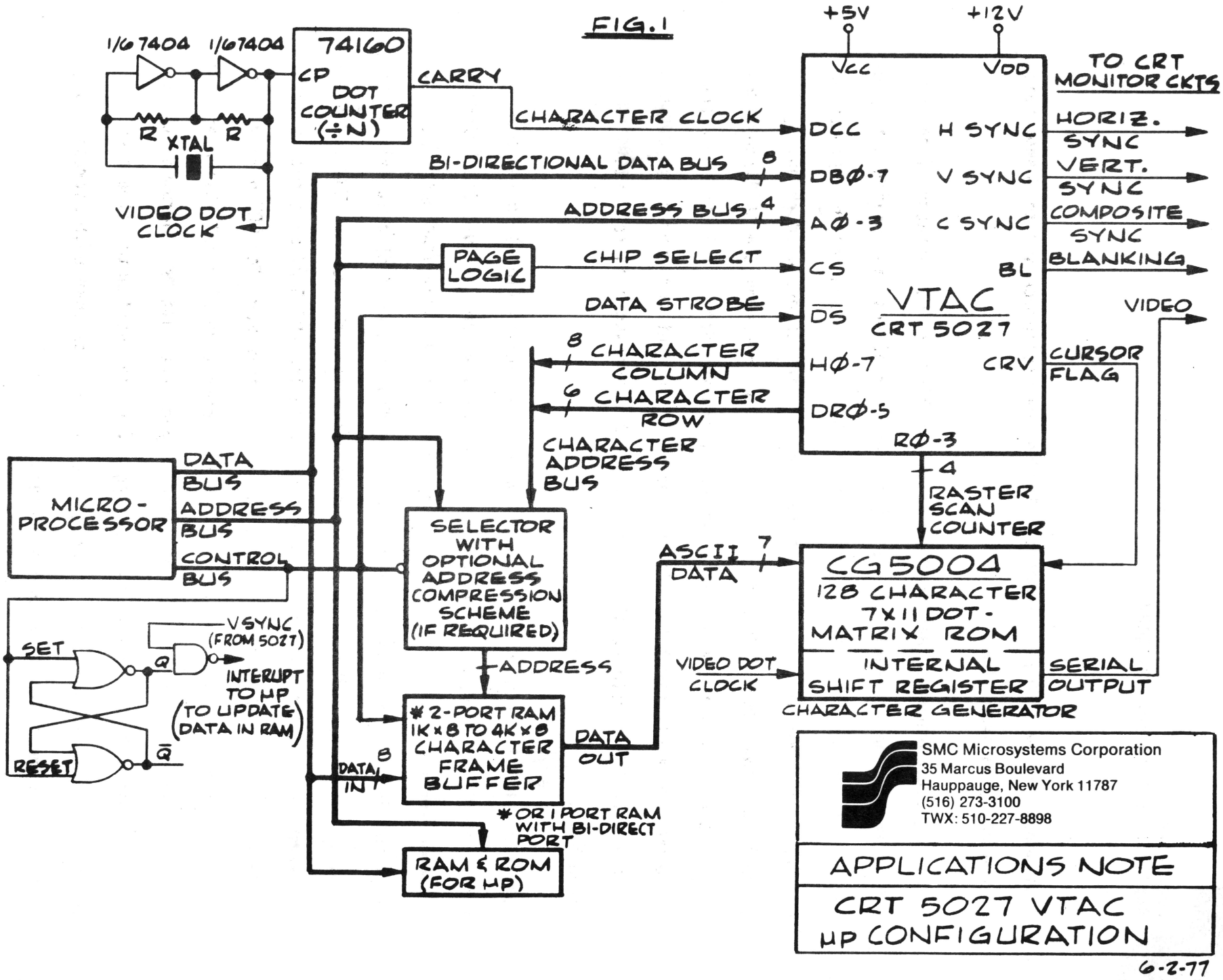
Whenever the data in the character frame buffer is to be changed or updated, the microprocessor (via the control bus) sets an external flip-flop. The output of this flip-flop is ANDed with the vertical sync signal from the VTAC. When this occurs an interrupt is generated to the microprocessor. This alerts the microprocessor to the fact that the vertical blanking interval has begun; it then switches the address selector (via control bus) so that the character frame buffer is now addressed by the microprocessor instead of the CRT 5027. Since the system is in the vertical blanking interval the screen is blank at this time. Using the American standard of 63.5 microseconds per horizontal line and a typical value of 21 horizontal lines for the blanking interval, this gives the system 1.33 milliseconds in which the microprocessor can change data in the character frame buffer. If this time is not sufficient the 1.33 millisecond window

will appear every 1/60 of a second; allowing the microprocessor to change part of the RAM data each time.

After the microprocessor has completed its updating of the character frame buffer RAM it resets the external flip-flop (via the control bus) and switches the selector back to the character address bus of the VTAC. Then the microprocessor goes about its normal system operation without being interrupted or having its throughput slowed down. This is because the VTAC refreshes the CRT independently with the character frame buffer RAM supplying the data. This method appears to be much more efficient for microprocessor throughput and control as opposed to having to DMA (cycle steal) or interrupt the processor; thereby reducing its throughput.

Some applications require adding alphanumeric characters (text) to the same screen as closed circuit or external (off-the-air) video. Figure 3 illustrates a simple technique of externally synchronizing the CRT 5027 VTAC using 2 chips (7474 and 7402). The external video can come from a closed circuit television system, off-the-air television, or another video display system. The technique involves stopping the character clock (DCC) when the CRT 5027 sync occurs and restarting it when the external sync occurs. In this way, the CRT 5027 will be synchronized to the external video. One requirement for the reliable operation of this system is that the VTAC horizontal sync rate must be programmed to be slightly faster than the external sync rate (ie. the horizontal line counter register of the CRT 5027 must be programmed to be less than 63.5 microseconds, which is the American TV horizontal rate).

FIG.1



SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

APPLICATIONS NOTE

CRT 5027 VTAC µP CONFIGURATION

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ADDRESS COMPRESSION SCHEME FOR 80 CHARACTERS/LINE

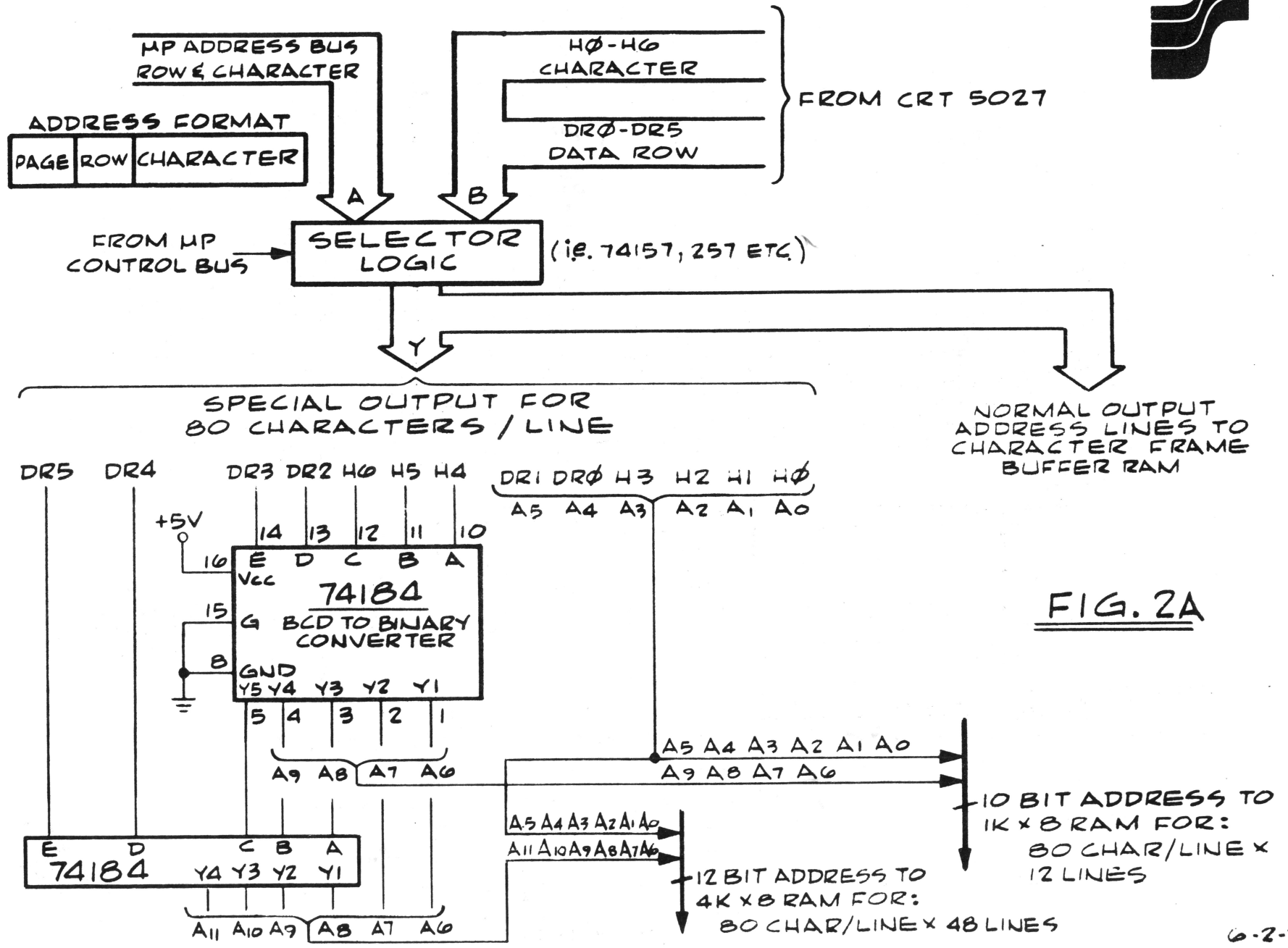

FIG. 2A

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MEMORY MAP

80 CHARACTERS/LINE X 12 LINES IN A 1K RAM
(USING A 74184 - BCD TO BINARY CONVERTER)

FOR GREATER THAN 12 LINES (1K) USE AN ADDITIONAL 74184
TO SELECT UP TO 48 LINES (4K)

EACH 64 BYTE SEGMENT IS 16 CHARACTERS X
4 LINES WITH ADDRESSING:

A5	A4	A3	A2	A1	A0
DR1	DR0	H3	H2	H1	H0

FRAME SEGMENT PARTITIONING

CHAR. / LINE	0 — 15	16 — 31	32 — 47	48 — 63	64 — 79	
0 — 3	A	B	C	D	E	0 0
4 — 7	F	G	H	I	J	0 1
8 — 11	K	L	M	N	O	1 0
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	DR3, DR2 / H6, H5, H4

74184 - BCD TO BINARY CONVERTER

		INPUT						OUTPUT			
		DR3	DR2	H6	H5	H4		A9	A8	A7	A6
ROW	CHAR.	E	D	C	B	A	SEG.	Y4	Y3	Y2	Y1
1K	0-3	0-15	0	0	0	0	0	A	0	0	0	0
	0-3	16-31	0	0	0	0	1	B	0	0	0	1
	0-3	32-47	0	0	0	1	0	C	0	0	1	0
	0-3	48-63	0	0	0	1	1	D	0	0	1	1
	0-3	64-79	0	0	1	0	0	E	0	1	0	0
	4-7	0-15	0	1	0	0	0	F	0	1	0	1
	4-7	16-31	0	1	0	0	1	G	0	1	1	0
	4-7	32-47	0	1	0	1	0	H	0	1	1	1
	4-7	48-63	0	1	0	1	1	I	1	0	0	0
	4-7	64-79	0	1	1	0	0	J	1	0	0	1
	8-11	0-15	1	0	0	0	0	K	1	0	1	0
	8-11	16-31	1	0	0	0	1	L	1	0	1	1
	8-11	32-47	1	0	0	1	0	M	1	1	0	0
	8-11	48-63	1	0	0	1	1	N	1	1	0	1
	8-11	64-79	1	0	1	0	0	O	1	1	1	0
	UNUSED (64 BYTES)						—	1	1	1	1

FIG. 2B

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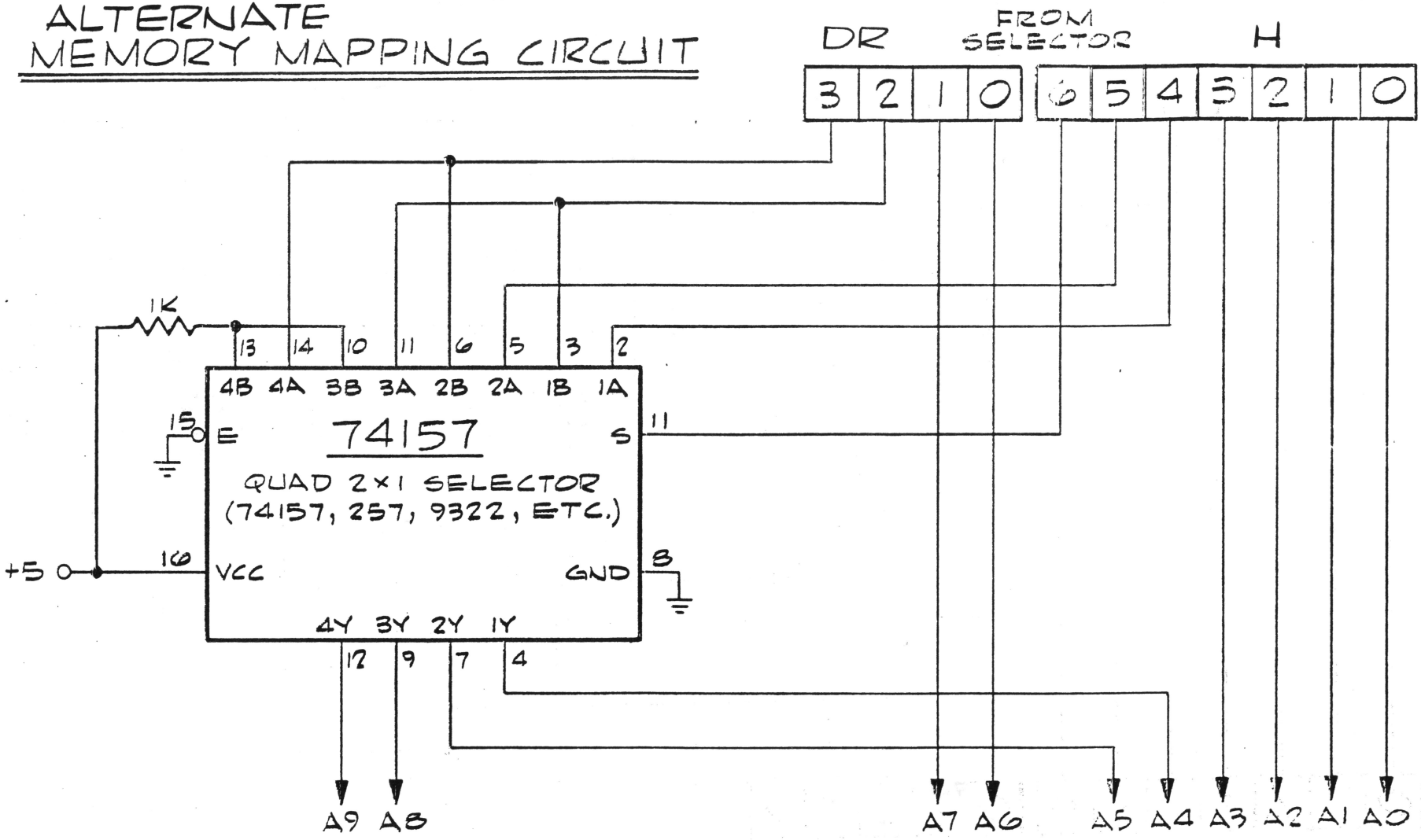
72 OR 80 CHARACTERS/LINE × 12 LINES INTO 1K BYTES

ALTERNATE MEMORY MAPPING CIRCUIT



10 BIT BINARY ADDRESS TO 1024 BYTE RAM

FIG 2C

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
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TWX: 510-227-8898

ORL
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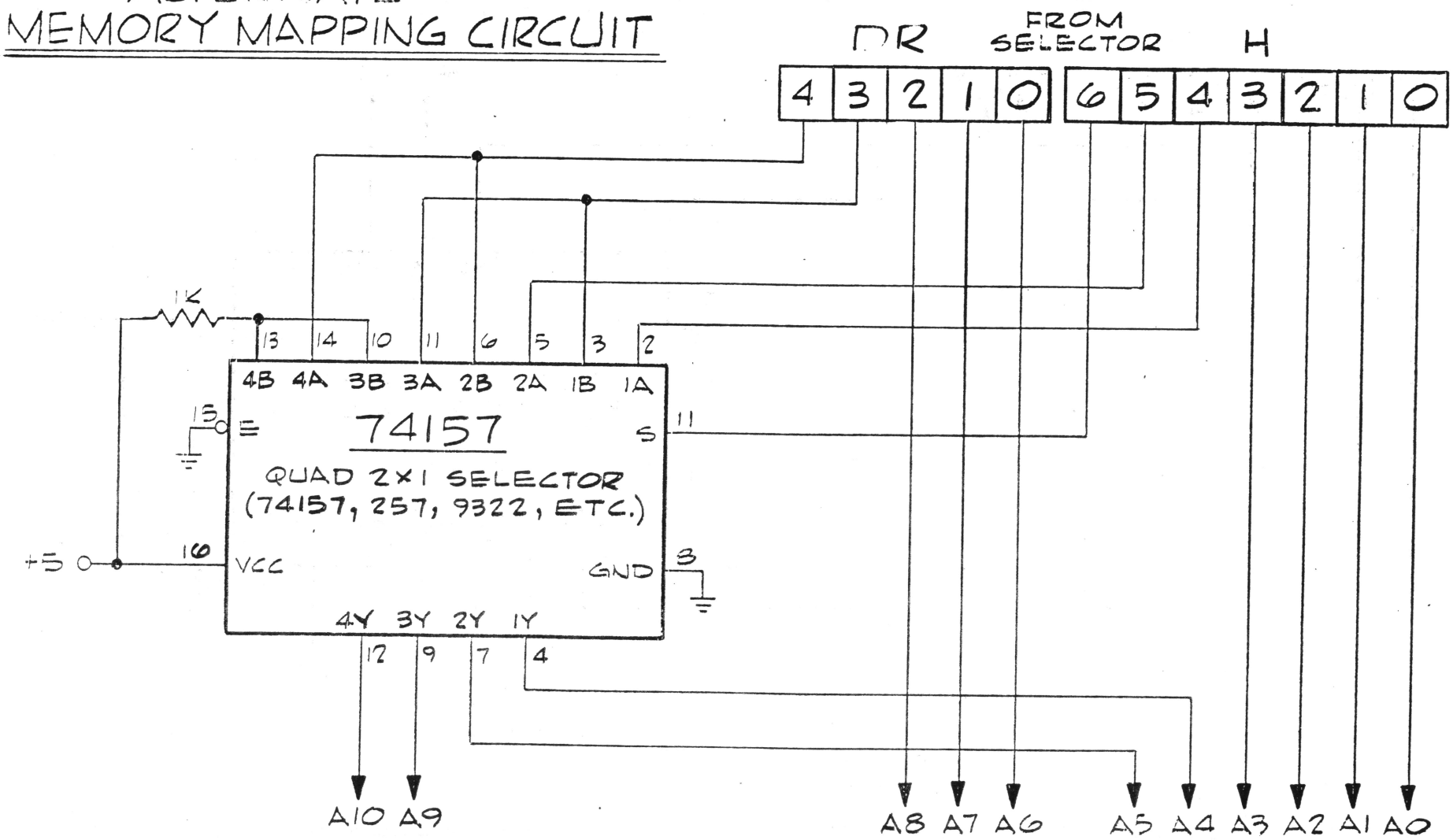
72 OR 80 CHARACTERS/LINE × 24 LINES INTO 2K BYTES

ALTERNATE MEMORY MAPPING CIRCUIT



11 BIT BINARY ADDRESS TO 2048 BYTE RAM

FIG. 2D

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Hauppauge, New York 11787
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DRL
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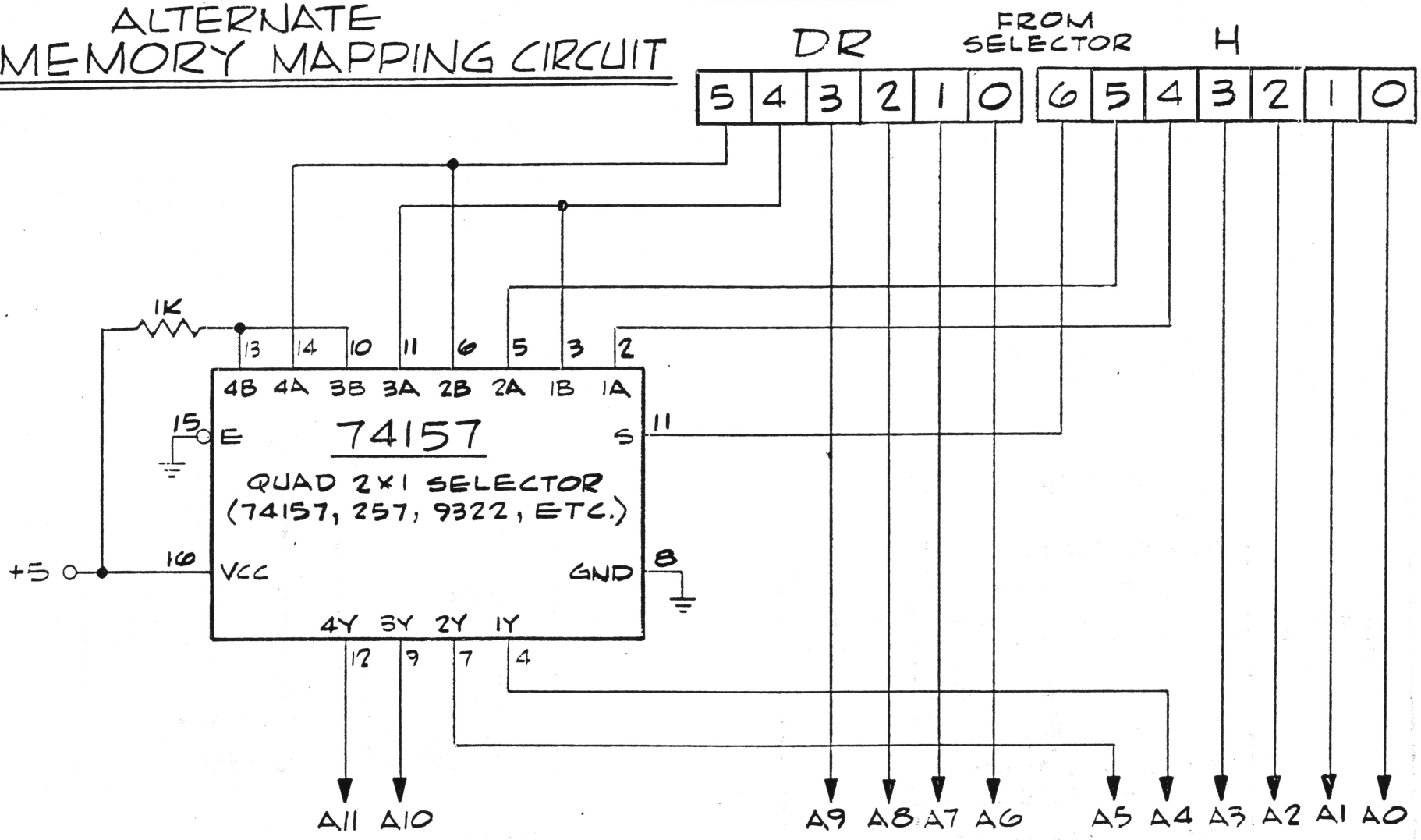
72 OR 80 CHARACTERS/LINE × 48 LINES INTO 4K BYTES

ALTERNATE MEMORY MAPPING CIRCUIT



12 BIT BINARY ADDRESS TO 4096 BYTE RAM

FIG 2E

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DRL

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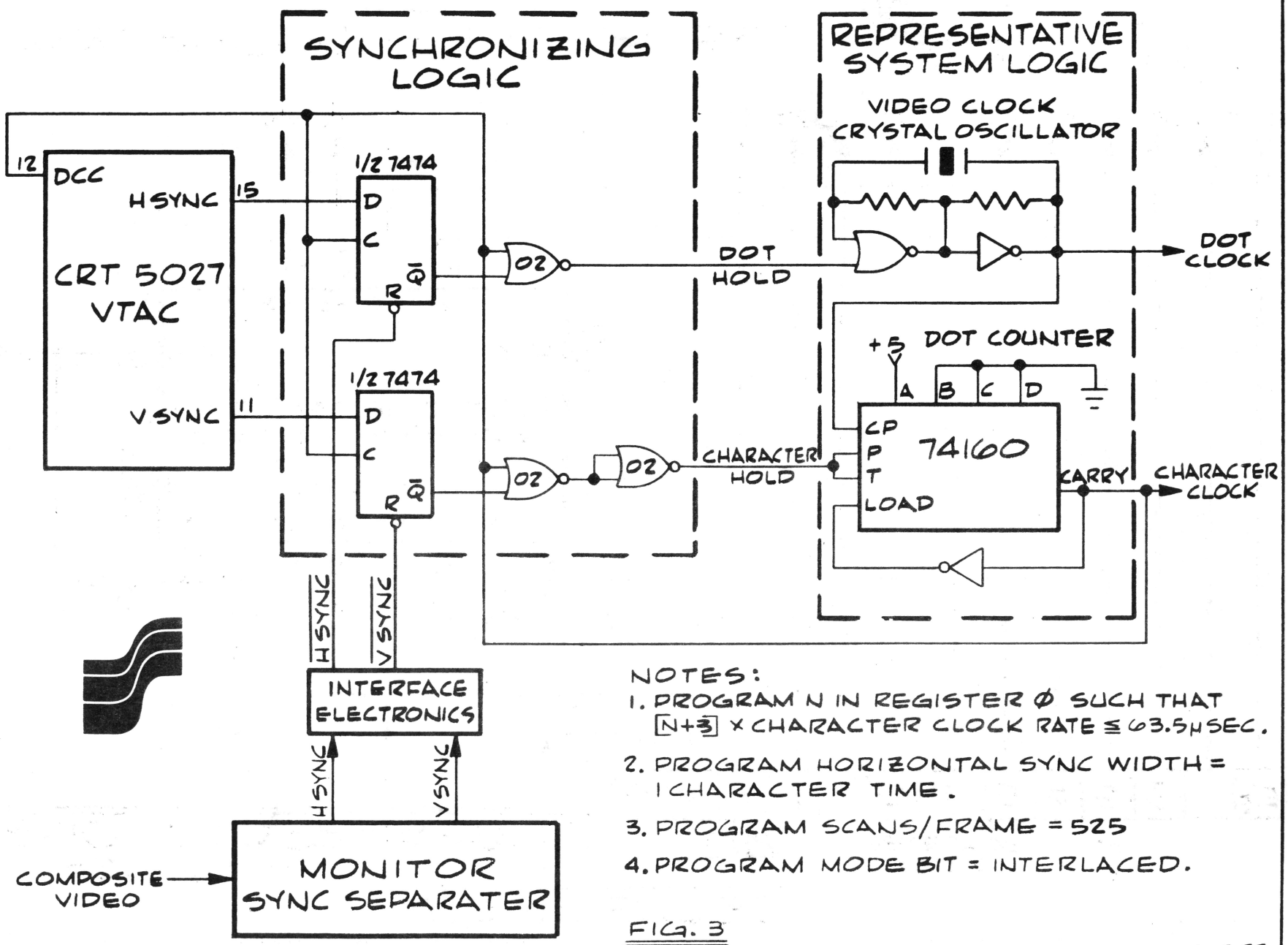
VTAC VIDEO OVERLAY SYNCHRONIZING CIRCUIT



NOTES:

1. PROGRAM N IN REGISTER Ø SUCH THAT [N+3] × CHARACTER CLOCK RATE ≥ 63.5μSEC.
2. PROGRAM HORIZONTAL SYNC WIDTH = 1 CHARACTER TIME.
3. PROGRAM SCANS/FRAME = 525
4. PROGRAM MODE BIT = INTERLACED.

FIG. 3

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CRT 5027

REVISED

ERRATA SHEET

The present revision CRT 5027 has two design anomalies:

1. The scan counter outputs (RØ, R1, R2, R3) on the present revision CRT 5027 count correctly, ie; from 0 to N, if and only if N (last scan per data row) is programmed as an even value. For N odd, the scan counter will count incorrectly from 1 to N. The result is that the device cannot produce an even number of raster scans per data row.

   Also, if the self load mode is desired, the CRT 5027 must first be given a Reset command prior to issuing either Self Load command.

   Revised product will not have this anomaly.

2. An incorrect waveform on the composite sync output in non-interlaced operation exists for certain combinations of the 4 least significant bits of Register Ø (horizontal line count) with respect to the programmed horizontal sync width (bits 3 - 6 of Register 1).

   The restrictions in programming of these two values required to produce a correct composite sync are listed in the table below.

Programmed Horizontal Line Count	Allowable Programmed Sync Width Values
Any even count	All
Four LSB's = 1, 5, 9, 13	All even values
= 3 or 11	4, 8, or 12
= 7	8 only
= 15	None

   Revised product will not have this anomaly.

3. Printing error on the data sheet; Register Selects/Command Codes should read:

A3	A2	A1	AØ	
1	0	0	0	Read Cursor LINE Address
1	0	0	1	Read Cursor CHARACTER Address

   This has been corrected on the new printing of the data sheet.

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